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leakage current, a low-power transistor can be provided. Additionally, as a small amount of silicon remains under the metallic silicide layers, a field effect transistor having a low resistance and a stable metallic silicide layer can be provided."

In the Claims:

The following replacement claims are respectfully submitted:

2. (Amended) The field effect transistor according to claim 1, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

3. (Amended) A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:
an insulating layer;
a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region therein;
a pair of impurity layers formed in regions which are respectively in contact with the channel region in the source region and the drain region; and
a pair of cobalt silicide layers respectively formed in the source region and the drain region, wherein the pair of cobalt silicide layers are respectively in contact with the pair of impurity layers, wherein bottom surfaces of the pair of cobalt silicide layers extend to bottom surfaces of the semiconductor layer;

wherein the cobalt silicide layers are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1 < \alpha < 2$).
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4. (Amended) The field effect transistor according to claim 3, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

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5. (Twice Amended) A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

- an insulating layer;
- a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region defined by the source region and the drain region;
- a pair of impurity layers formed into regions which are respectively in contact with the channel region in the source region and the drain region; and
- a pair of metallic silicide layers respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers are respectively in contact with the pair of impurity layers, wherein the pair of metallic silicide layers have a thickness which is equal to or more than 80% thickness of from an upper surface of the metallic silicide layers to a bottom surface of the semiconductor layer;

wherein the metallic silicide layers are composed of refractory metal and silicon,
and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a
ratio of the metal to the silicon of metallic silicide having the lowest resistance among
stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following
inequality:

$$(X / Y) > (X_0 / Y_0).$$

6. (Amended) The field effect transistor according to claim 5, wherein said field
effect transistor has a depletion layer which expands to bottom surfaces of the source
region and the drain region when a voltage is supplied to the gate electrode thereof.

7. (Amended) A field effect transistor including a gate electrode and a channel
region defined by a source region and a drain region, comprising:
an insulating layer;
a semiconductor layer formed on the insulating layer, wherein the semiconductor
layer includes the channel region therein;
a pair of impurity layers formed in regions which are respectively in contact with
the channel region in the source region and the drain region; and
a pair of cobalt silicide layers respectively formed in the source region and the
drain region, wherein the pair of cobalt silicide layers are respectively in contact with the

pair of impurity layers, wherein the pair of cobalt silicide layers has a thickness which is equal to or more than 80% thickness of from an upper surface of the cobalt silicide layers to a bottom surface of the semiconductor layer;

wherein the cobalt silicide layers are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1 < \alpha < 2$).

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8. (Amended) The field effect transistor according to claim 7, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

10. (Amended) The field effect transistor according to claim 9, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to a gate electrode thereof.

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11. (Amended) A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first cobalt silicide layer, wherein the first impurity layer and the first cobalt silicide layer are formed so as to reach the insulating layer through the semiconductor layer; and

the drain region including a second impurity layer and a second cobalt silicide layer, wherein the second impurity layer and the second cobalt silicide layer are formed so as to reach the insulating layer through the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity layer and the second impurity layer, and

wherein the first cobalt silicide layer and the second cobalt silicide layer are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to a ($1 < \alpha < 2$).

12. (Amended) The field effect transistor according to claim 11, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to a gate electrode thereof.

14. (Amended) The field effect transistor according to claim 13, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to a gate electrode thereof.

15. (Amended) A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first cobalt silicide layer, wherein the first cobalt silicide layer has a thickness which is equal to or more than 80% thickness of from an upper surface of the first cobalt silicide layer to a bottom surface of the semiconductor layer; and

the drain region including a second impurity layer and a second cobalt silicide layer, wherein the second cobalt silicide layer has a thickness which is equal to or more than 80% thickness of from an upper surface of the second cobalt silicide layer to a bottom surface of the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity layer and the second impurity layer, and

wherein the first cobalt silicide layer and the second cobalt silicide layer are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to a ($1 < a < 2$).

16. (Amended) The field effect transistor according to claim 15, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the

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source region and the drain region when a voltage is supplied to a gate electrode
thereof.

Please add claims 23-30 as follows:

--23. The field effect transistor according to claim 1, wherein a contact specific
resistance between the metallic silicide layers and the impurity layers is less than
 $1 \times 10^{-7} \Omega - \text{cm}^2$.

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24. The field effect transistor according to claim 3, wherein a contact specific
resistance between the cobalt silicide layers and the impurity layers is less than
 $1 \times 10^{-7} \Omega - \text{cm}^2$.

25. The field effect transistor according to claim 5, wherein a contact specific
resistance between the metallic silicide layers and the impurity layers is less than
 $1 \times 10^{-7} \Omega - \text{cm}^2$.

26. The field effect transistor according to claim 7, wherein a contact specific
resistance between the cobalt silicide layers and the impurity layers is less than
 $1 \times 10^{-7} \Omega - \text{cm}^2$.

27. The field effect transistor according to claim 9, wherein a first contact specific resistance between the first metallic silicide layer and the first impurity layer, and a second contact specific resistance between the second metallic silicide layer and the second impurity layer, are less than $1 \times 10^{-7} \Omega \text{ - cm}^2$.

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28. The field effect transistor according to claim 11, wherein a first contact specific resistance between the first cobalt silicide layer and the first impurity layer, and a second contact specific resistance between the second cobalt silicide layer and the second impurity layer, are less than $1 \times 10^{-7} \Omega \text{ - cm}^2$.

29. The field effect transistor according to claim 13, wherein a first contact specific resistance between the first metallic silicide layer and the first impurity layer, and a second contact specific resistance between the second metallic silicide layer and the second impurity layer, are less than $1 \times 10^{-7} \Omega \text{ - cm}^2$.

30. The field effect transistor according to claim 15, wherein a first contact specific resistance between the first cobalt silicide layer and the first impurity layer, and a second contact specific resistance between the second cobalt silicide layer and the second impurity layer, are less than $1 \times 10^{-7} \Omega \text{ - cm}^2$.--